Amendments To The Claims

Claim 1 (currently amended): A system comprising:

a first processor including a first processor data channel;

a first hybrid switching module including a first hybrid switching module processor data channel, a first hybrid switching module main data channel, a first input/output link data channel, a first crossbar switch and arbiter, and a first bridge, the first hybrid switching module processor data channel being coupled to the first processor data channel;

a first main bus coupled to the first hybrid switching module main data channel allowing the first processor to access a first peripheral device coupled with the first main bus to implement a first function;

a second processor including a second processor data channel; [[and]]

a second hybrid switching module including a second hybrid switching module processor data channel, a second hybrid switching module main data channel, a second input/output link data channel, a second crossbar switch and arbiter, and a second bridge, the second hybrid switching module processor data channel being coupled to the second processor data channel, the second input/output link data channel being coupled to the first input/output link data channel; and

a second main bus coupled to the second hybrid switching module main data channel allowing the second processor to access a second peripheral device coupled with the second main bus to implement a second function that is not redundant to the first function;

wherein the first hybrid switching module further comprises a failure mode that couples the first input/output link data channel with the first main bus when the first processor fails allowing the second processor to access the first peripheral device on the first main bus to implement the first function, and the second hybrid switching module further comprises a failure mode that couples the second input/output link data channel with the second main bus when the second processor fails allowing the first processor to access the second peripheral device on the second main bus to implement the second non-redundant function.

Claim 2 (cancelled)

Claim 3 (original): The system of Claim 1 further comprising:

a third processor including a third processor data channel; and

a third hybrid switching module including a third hybrid switching module processor data channel, a third input/output link data channel, a fourth input/output link data channel, and a third switch, the third hybrid switching module processor data channel being coupled to the third processor data channel;

wherein said first hybrid switching module further comprises a fifth input/output link data channel;

wherein the third input/output link data channel is coupled to the fifth input/output link data channel;

wherein said second hybrid switching module further comprises a sixth input/output link data channel;

wherein the fourth input/output link data channel is coupled to the sixth input/output link data channel.

Claim 4 (cancelled)

Claim 5 (currently amended): The system of Claim [[4]] 3 wherein said third hybrid switching module further comprises a third hybrid switching module main data channel, wherein said system further comprises:

a third main bus coupled to the ~~second~~ third hybrid switching module main data channel.

Claim 6 (currently amended): An apparatus comprising:

a first hybrid switching module comprising:

a first hybrid switching module processor data channel;

a first hybrid switching module main data channel;

an input/output link data channel;

a first switch coupled to the first hybrid switching module processor data channel; and

a first bridge coupled to the first hybrid switching module main data channel;

wherein the first switch selectively couples to the first bridge and selectively couples to the input/output link data channel, wherein the first hybrid switching module processor data channel is thereby selectively coupled to the first bridge allowing access over a first main bus to a first peripheral device that implements a first function, and selectively coupled to the input/output link data channel allowing access over a second main bus to a second peripheral device that implement a second function that is not redundant to the first function.

Claim 7 (previously presented): The apparatus of Claim 6 further comprising a first processor coupled to the first hybrid switching module processor data channel.

Claim 8 (currently amended): The apparatus of Claim 6 ~~further comprising~~ a, wherein the first main bus is coupled to the first bridge.

Claim 9 (previously presented): The apparatus of Claim 6 further comprising a second switch coupled to the input/output link data channel.

Claim 10 (previously presented): The apparatus of Claim 9 further comprising second bridge coupled to the second switch.

Claim 11 (currently amended): The apparatus of Claim 10 further comprising:

[[a]] the first main bus is coupled to the first bridge; and

[[a]] the second main bus is coupled to the second bridge.

Claim 12 (previously presented): The apparatus of Claim 9 further comprising:

a first processor coupled to the first hybrid switching module processor data channel; and

a second processor coupled to a second hybrid switching module processor data channel, the second switch being coupled to the second hybrid switching module processor data channel.

Claim 13 (currently amended): A system comprising:

a first hybrid switching module processor data channel;

a first hybrid switching module main data channel;

a first hybrid switching module bus data channel;

an input/output link data channel; and

a first hybrid switching module coupled to the first hybrid switching module processor data channel and to the first hybrid switching module main data channel;

wherein the first hybrid switching module selectively couples to the first hybrid switching module bus data channel and selectively couples to the input/output link data channel, wherein the first hybrid switching module processor data channel is thereby selectively coupled to the first hybrid switching module bus data channel allowing access to a first peripheral device providing a first function, and selectively coupled to the input/output link data channel allowing access to a second peripheral device providing a second function that is not redundant of the first function, and the first hybrid switching module further comprises a failure mode that couples the input/output link data channel with the first hybrid switching module bus data channel during a failure allowing external access to the first peripheral device providing the first function during the failure.

Claim 14 (previously presented): The apparatus of Claim 13 further comprising a first processor coupled to the first hybrid switching module processor data channel.

Claim 15 (previously presented): The apparatus of Claim 13 further comprising a first main bus coupled to the first hybrid switching module bus data channel.

Claim 16 (previously presented): The apparatus of Claim 13 further comprising a second hybrid switching module coupled to the input/output link data channel.

Claim 17 (previously presented): The apparatus of Claim 16 further comprising:

a first main bus coupled to the first hybrid switching module; and

a second main bus coupled to the second hybrid switching module.

Claim 18 (currently amended): The apparatus of Claim 16 further comprising:

a first processor coupled to the first hybrid switching module processor data channel; and

a second processor coupled to a second hybrid switching module processor data channel, the second hybrid switching module being coupled to the second hybrid switching module processor data channel such that the second processor has access to the first function of the first peripheral device through the input/output link data channel at least during the failure.